

Appl. No. 10/063,772

Amdt. dated January 18, 2005

Reply to Office action of October 18, 2004

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for determining an operating
5 voltage of floating point error detection of a central
processing unit (CPU) through a ~~control circuit~~ south bridge
chipset; said CPU comprising a first output port, wherein said
first output port is floating when said operating voltage of
floating point error detection of said CPU is higher than a
10 first predetermined voltage level, and said first output port
is connected to a grounding when said operating voltage of
floating point error detection of said CPU is lower than said
first predetermined voltage level; said ~~control circuit~~ south
bridge chipset comprising a test port connected to the first
15 output port of said CPU for determining said operating voltage
of floating point error detection of said CPU;
said method comprising:
providing a power supply connected to the first output port
of said CPU via a resistor for supplying a first voltage
20 level; and
measuring a voltage level at said test port of said ~~control
circuit~~ south bridge chipset to determine said
operating voltage of floating point error detection of
said CPU.
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2. (currently amended) The method of claim 1 wherein said first
voltage level is a positive voltage, said operating voltage
of said CPU is higher than said first predetermined voltage
level when said voltage level at said test port of said ~~control
circuit~~ south bridge chipset is higher than a second
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predetermined voltage level, and said operating voltage of
said CPU is lower than said first predetermined voltage level
when said voltage level at said test port of said ~~control-~~
5 ~~circuit~~ south bridge chipset is lower than said second
predetermined voltage level.

3. (cancelled)

10 4. (currently amended) The method of claim 1 wherein said CPU
further comprises a second output port connected to a signal
input port of said ~~control circuit~~ south bridge chipset for
transmitting a predetermined signal;

said method further comprising:

15 determining information contained in said predetermined
signal according to said operating voltage of floating
point error detection of said CPU.

20 5. (original) The method of claim 4 wherein said predetermined
signal is a floating point error signal (FERR#) of said CPU.

25 6. (new) A method for determining an operating voltage of floating
point error detection of a central processing unit (CPU)
through a control circuit; said CPU comprising a first output
port, wherein said first output port is floating when said
operating voltage of floating point error detection of said
CPU is higher than a first predetermined voltage level, and
said first output port is connected to a grounding when said
operating voltage of floating point error detection of said
30 CPU is lower than said first predetermined voltage level; said

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CPU further comprising a second output port connected to a signal input port of said control circuit for transmitting a predetermined signal; said control circuit comprising a test port connected to the first output port of said CPU for determining said operating voltage of floating point error detection of said CPU;

said method comprising:

providing a power supply connected to the first output port of said CPU via a resistor for supplying a first voltage level;

measuring a voltage level at said test port of said control circuit to determine said operating voltage of floating point error detection of said CPU; and

determining information contained in said predetermined signal according to said operating voltage of floating point error detection of said CPU.

7. (new) The method of claim 6 wherein said first voltage level is a positive voltage, said operating voltage of said CPU is higher than said first predetermined voltage level when said voltage level at said test port of said control circuit is higher than a second predetermined voltage level, and said operating voltage of said CPU is lower than said first predetermined voltage level when said voltage level at said test port of said control circuit is lower than said second predetermined voltage level.

8. (new) The method of claim 6 wherein said control circuit is a south bridge chipset.

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9. (new) The method of claim 6 wherein said predetermined signal is a floating point error signal (FERR#) of said CPU.